REMARKS

The applicants note with appreciation the acknowledgement of the claim for priority under section 119 and the notice that all of the certified copies of the priority documents have been received in the parent application.

Also, the applicants appreciate receiving an initialed copy of the forms PTO-1449 that were filed on November 20, 2003, September 7, 2004 and August 2, 2005.

Claims 1 – 3, 5 and 15 – 32 are pending. Claim 4 has been canceled. Claims 5 and 15 – 29 have been withdrawn. The applicants respectfully request reconsideration and allowance of this application in view of the above amendments and the following remarks.

Claims 1 – 2 and 4 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 5,611,855, Wijaranakula ("Wijaranakula"). Claim 1 has been amended to incorporate claim 4, and claim 4 is canceled. Claim 3 was rejected under 35 USC 103(a) as being unpatentable over Wijaranakula. The rejections are respectfully traversed for reasons including the following, which are provided by way of example.

Claim 1 recites in combination, for example, forming an epitaxial layer on a semiconductor substrate by epitaxial growth; and forming an insulating layer by deposition at an interface between the epitaxial layer and the semiconductor substrate by performing a heat treatment that is performed in an oxidizing atmosphere, wherein the heat treatment for forming the insulating layer is performed at a temperature higher than about 1000° C. Consequently, the insulating layer made of oxides is formed at the interface from a distortion layer of the interface as nuclei. Since the interface is disposed to be stratiform, the insulating layer also becomes stratiform.

Without conceding that Wijaranakula discloses any feature of the present invention, Wijaranakula is directed to a method for manufacturing a calibration wafer having a microdefect-free layer of precisely predetermined depth. According to Wijaranakula, the wafer is annealed at a suitable temperature to nucleate microdefects (Fig. 4, step 48), "preferably between 600°C and 900°C and more preferably between 650°C and 750°C" (column 5, line 36 - 37). Therefore, the nucleating step in Wijaranakula is performed at a comparatively low temperature for longer than 24 hours (Col. 5, lines 33 – 50).

The office action asserts that Wijaranakula discloses the invention as claimed. To the contrary, Wijaranakula fails to teach or suggest the invention, as presently claimed, when the claims are considered as a whole.

In operation, the distortion layer according to independent claim 1 is formed at the interface by a difference of impurity concentration between the epitaxial layer and the semiconductor substrate, specifically, the difference of oxygen concentration. Alternatively, the distortion layer can be formed by a difference of dopant concentration or a difference of a lattice constant between the epitaxial layer and the semiconductor substrate.

According to Wijaranakula, a method for forming a micro-defect includes two steps, one of which is a step (48) of nucleating the micro-defect and the other step is growing (50) the micro-defect. The office action equates the recited insulating layer to the micro-defect (14) in Wijaranakula.

Wijaranakula, however, fails to teach or suggests, for example, forming the insulating layer as recited. To the contrary, the micro-defect layer (30) of Wijanarakula is not disclosed to be an insulating layer. More specifically, Wijaranakula fails to teach or suggest that the micro-

defect is layered. To the contrary, the micro-defect concentration is uniform throughout the substrate (Col. 5, lines 10 – 22, 47 – 50).

Thus, in Wijaranakula, the calibration wafer (10) is manufactured with the epitaxial layer (16) without micro-defect and the substrate with micro-defects disposed uniformly. On the other hand, as recited, the semiconductor substrate has the epitaxial layer, the insulating layer (e.g., the stratiform region), and the semiconductor substrate, which are stacked in that order.

Moreover, according to Wijaranakula, the nucleating step has a comparatively low process temperature (i.e., between 600°C and 900°C) and the growing step has a comparatively high process temperature (i.e., between 850°C and 1200°C). To the contrary, claim 1 recites, in combination, forming an insulating layer by performing a heat treatment, the heat treatment for forming the insulating layer being performed at a temperature higher than about 1100°C.

Wijaranakula fails to teach or suggest, for example, these elements recited in independent claim 1. It is respectfully submitted therefore that claim 1 is patentable over Wijaranakula.

For at least these reasons, the combination of features recited in independent claim 1, when interpreted as a whole, is submitted to patentably distinguish over the prior art. In addition, Wijaranakula clearly fails to show other recited elements as well.

With respect to the rejected dependent claims, applicants respectfully submit that these claims are allowable not only by virtue of their dependency from independent claim 1, but also because of additional features they recite in combination.

New claims 30 – 32 have been added to further define the invention, and are believed to be patentable for reasons including these set out above. Support for claims 30 – 32 is located in the specification as filed, for example, page 6, line10 – page 7, line 20; page 7, lines 7 – 14; and page 7, lines 14 – 16.

Applicants respectfully submit that, as described above, the cited prior art does not show or suggest the combination of features recited in the claims. Applicants do not concede that the cited prior art shows any of the elements recited in the claims. However, applicants have provided specific examples of elements in the claims that are clearly not present in the cited prior art.

Applicants strongly emphasize that one reviewing the prosecution history should not interpret any of the examples applicant has described herein in connection with distinguishing over the prior art as limiting to those specific features in isolation. Rather, for the sake of simplicity, applicants have provided examples of why the claims described above are distinguishable over the cited prior art.

In view of the foregoing, the applicants submit that this application is in condition for allowance. A timely notice to that effect is respectfully requested. If questions relating to patentability remain, the examiner is invited to contact the undersigned by telephone.

If there are any problems with the payment of fees, please charge any underpayments and credit any overpayments to Deposit Account No. 50-1147.

Respectfully submitted,

Cynthia K. Nicholson
Reg. No. 36,880

Posz Law Group, PLC
12040 South Lakes Drive, Suite 101
Reston, VA 20191
Phone 703-707-9110
Fax 703-707-9112
Customer No. 23400